

## ISL7457SRH TID Rating

The ISL7457SRH is specified for 10krads(Si) minimum TID in SMD 5962-08230 when continuously biased as shown in Figure 1.

In many cases a 10krad(Si) TID rating is not adequate to meet mission requirements, so a method to extend the TID capability is desired. Figure 2 shows a radiation exposure circuit that biases the ISL7457SRH only 20% of the time. For the other 80% of the time, the ISL7457SRH is unbiased. Devices irradiated in this manner have demonstrated acceptable post-rad parametric limits after 50krad(Si) TID, as indicated in the Electrical Specification tables of this application note. Please note, however, that the post-50krad electrical specifications shown herein are not specified in or guaranteed by SMD 5962-08230.

## Imaging Applications

Some camera CCD driver applications do not require 100% availability. In these situations, the ISL7457SRH can be left unbiased until there is a need to image. When imaging is required, the ISL7457SRH can be quickly biased by simply closing a switch. As long as the duty-cycle of the application does not exceed 20%, the TID capability can be extended up to 50krad(Si).

## Conclusions

A simple method to extend the TID capability of the ISL7457SRH to 50krad(Si) has been described. This method can be applied to any space-based system that uses the device as long as 20% availability is acceptable.

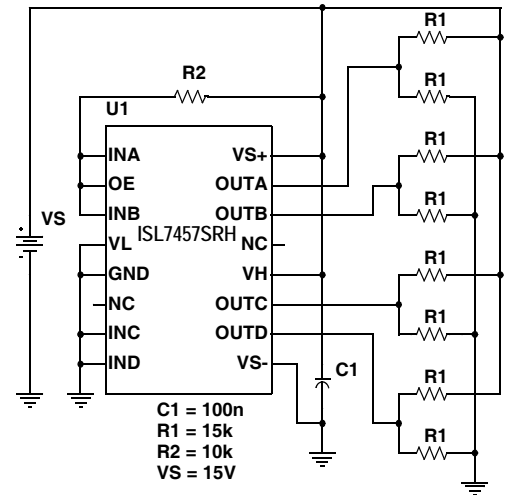


FIGURE 1. RAD EXPOSURE CIRCUIT (BIAS DUTY CYCLE = 100%)

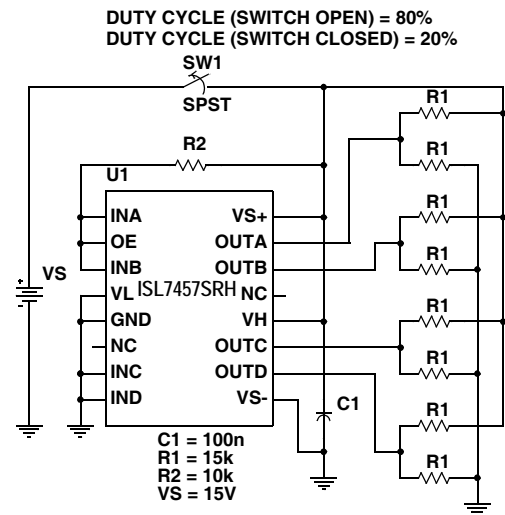


FIGURE 2. RAD EXPOSURE CIRCUIT (BIAS DUTY CYCLE = 20%)

## Application Note 1458

**Electrical Specifications**  $V_{S+} = V_H = 5V \pm 10\%$ ,  $V_{S-} = V_L = 0V$ ,  $OE = V_{S+}$ ,  $T_A = +25^\circ C$ , Post 50krad(Si) unless otherwise specified. Refer to Figure 2 for radiation exposure circuit biasing.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
<b>INPUT</b>						
$V_{IH}$	Logic "1" Input Voltage		2			V
$I_{IH}$	Logic "1" Input Current	$INx = V_{S+}$	-10		10	$\mu A$
$V_{IL}$	Logic "0" Input Voltage				0.6	V
$I_{IL}$	Logic "0" Input Current	$INx = 0V$	-10		10	$\mu A$
<b>OUTPUT</b>						
$R_{OH}$	ON Resistance $V_H$ to $OUTx$	$INx = V_{S+}$ , $I_{OUTx} = -100mA$			12	$\Omega$
$R_{OL}$	ON Resistance $V_L$ to $OUTx$	$INx = 0V$ , $I_{OUTx} = +100mA$			7	$\Omega$
$I_{LEAK+}$	Positive Output Leakage Current	$INx = V_{S+}$ , $OE = 0V$ , $OUTx = V_{S+}$			300	$\mu A$
$I_{LEAK-}$	Negative Output Leakage Current	$INx = V_{S+}$ , $OE = 0V$ , $OUTx = V_{S-}$	-50			$\mu A$
<b>POWER SUPPLY</b>						
$I_{S+}$	$V_{S+}$ Supply Current	$INx = 0V$ and $V_{S+}$			5	mA
$I_{S-}$	$V_{S-}$ Supply Current	$INx = 0V$ and $V_{S+}$	-5			mA
$I_H$	$V_H$ Supply Current	$INx = 0V$ and $V_{S+}$			650	$\mu A$
$I_L$	$V_L$ Supply Current	$INx = 0V$ and $V_{S+}$	-650			$\mu A$
<b>SWITCHING CHARACTERISTICS</b>						
$t_R$	Rise Time	$INx = 0V$ to 4.5V step, $C_L = 1nF$			40	ns
$t_F$	Fall Time	$INx = 4.5V$ to 0V step, $C_L = 1nF$			26	ns
$t_{RFA}$	$t_R$ , $t_F$ Mismatch	$C_L = 1nF$			5	ns
$t_{D+}$	Turn-On Delay Time	$INx = 0V$ to 4.5V step, $C_L = 1nF$			30	ns
$t_{D-}$	Turn-Off Delay Time	$INx = 4.5V$ to 0V step, $C_L = 1nF$			40	ns
$t_{DD}$	$t_{D+}$ , $t_{D-}$ Mismatch	$C_L = 1nF$			12	ns
$t_{ENABLE}$	Enable Delay Time	$INx = V_{S+}$ , $OE = 0V$ to 4.5V step, $R_L = 1k\Omega$			35	ns
$t_{DISABLE}$	Disable Delay Time	$INx = V_{S+}$ , $OE = 4.5V$ to 0V step, $R_L = 1k\Omega$			50	ns

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**Electrical Specifications**  $V_{S+} = V_H = 15V \pm 10\%$ ,  $V_{S-} = V_L = 0V$ ,  $OE = V_{S+}$ ,  $T_A = +25^\circ C$ , Post 50krad(Si) unless otherwise specified.  
Refer to Figure 2 for radiation exposure circuit biasing.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
<b>INPUT</b>						
$V_{IH}$	Logic "1" Input Voltage		2			V
$I_{IH}$	Logic "1" Input Current	$INx = V_{S+}$	-10		10	$\mu A$
$V_{IL}$	Logic "0" Input Voltage				0.6	V
$I_{IL}$	Logic "0" Input Current	$INx = 0V$	-10		10	$\mu A$
<b>OUTPUT</b>						
$R_{OH}$	ON Resistance $V_H$ to $OUTx$	$INx = V_{S+}$ , $I_{OUTx} = -100mA$			5	$\Omega$
$R_{OL}$	ON Resistance $V_L$ to $OUTx$	$INx = 0V$ , $I_{OUTx} = +100mA$			5	$\Omega$
$I_{LEAK+}$	Positive Output Leakage Current	$INx = V_{S+}$ , $OE = 0V$ , $OUTx = V_{S+}$			300	$\mu A$
$I_{LEAK-}$	Negative Output Leakage Current	$INx = V_{S+}$ , $OE = 0V$ , $OUTx = V_{S-}$	-50			$\mu A$
<b>POWER SUPPLY</b>						
$I_{S+}$	$V_{S+}$ Supply Current	$INx = 0V$ and $V_{S+}$			5	mA
$I_{S-}$	$V_{S-}$ Supply Current	$INx = 0V$ and $V_{S+}$	-5			mA
$I_H$	$V_H$ Supply Current	$INx = 0V$ and $V_{S+}$			750	$\mu A$
$I_L$	$V_L$ Supply Current	$INx = 0V$ and $V_{S+}$	-750			$\mu A$
<b>SWITCHING CHARACTERISTICS</b>						
$t_R$	Rise Time	$INx = 0V$ to $5V$ step, $C_L = 1nF$			20	ns
$t_F$	Fall Time	$INx = 5V$ to $0V$ step, $C_L = 1nF$			20	ns
$t_{RF\Delta}$	$t_R$ , $t_F$ Mismatch	$C_L = 1nF$			3	ns
$t_{D+}$	Turn-On Delay Time	$INx = 0V$ to $5V$ step, $C_L = 1nF$			20	ns
$t_{D-}$	Turn-Off Delay Time	$INx = 5V$ to $0V$ step, $C_L = 1nF$			20	ns
$t_{DD}$	$t_{D+}$ , $t_{D-}$ Mismatch	$C_L = 1nF$			5	ns
$t_{ENABLE}$	Enable Delay Time	$INx = V_{S+}$ , $OE = 0V$ to $5V$ step, $R_L = 1k\Omega$			25	ns
$t_{DISABLE}$	Disable Delay Time	$INx = V_{S+}$ , $OE = 5V$ to $0V$ step, $R_L = 1k\Omega$			65	ns

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

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